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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/681,577 | 10/07/2003 | Christopher J. Diorio | IMPJ-0004<br>033327-000036 | 6797 |

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THELEN REID & PRIEST LLP
IMPJ
P.O. BOX 640640
SAN JOSE, CA 95164-0640

| EXAMINER | |
|---|---|
| NGUYEN, HAI L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/681,577 | DIORIO ET AL. | |
| | Examiner | Art Unit | |
| | Hai L. Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-32,35-44 and 47-51* is/are pending in the application.

4a) Of the above claim(s) *18-26* is/are withdrawn from consideration.

5)☒ Claim(s) *1-17,27-32,47 and 48* is/are allowed.

6)☒ Claim(s) *35,36 and 41* is/are rejected.

7)☒ Claim(s) *37-40,42-44 and 49-51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/21/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Election*

1. Applicant's affirmation of the election received on 3/18/05 is acknowledged. However, this application still contains non-elected claims 18-26. Therefore, a complete reply to this Office Action must include cancellation of those non-elected claims.

### *Response to Amendment*

2. The amendment received on 3/18/05 has been reviewed and considered with the following results:

As to the objection to the drawings, Applicant's revision of the drawings has overcome the objection by the previous office action mailed on 12/16/2004, as such; the objection has been withdrawn. However, there is still similar problem in the drawings.

As to the objections to the specification, Applicant's amendments have overcome the objections, as such; the objections have been withdrawn.

As to the rejection to claim 12, under 35 U.S.C. 112, 2nd paragraph, Applicant's amendments of the claims have overcome the rejections, as such; the rejections have been withdrawn.

As to the prior art rejections to the claims made in the previous Office Action are now withdrawn in view of Applicant's amendments. However, Applicant's amendments necessitate new ground of rejection as set forth below.

### *Drawings*

3. Figures 6A-6C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

4. Claims 37-40, 42-44, and 49-51 are objected to because of the following informalities: dependent on the base claims, which have been canceled. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 41 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the clear necessary structural connections between an analog-to-digital converter and other elements of the signal processing apparatus recited in claim 35.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 35 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Hui at al. (US 5,933,039; IDS).

With regard to claim 35, Hui et al. discloses in Figs. 1a-2a a signal processing apparatus, comprising an electrical circuit (100); and a floating-gate field effect transistor (231-238) disposed in a first circuit (108) pathway of the circuit, wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit (128) characteristic in a second circuit pathway of the circuit, wherein the first and second circuit characteristics correspond to relative gains of circuit elements in the first and second circuit pathways.

With regard to claim 36, Hui et al. discloses in Figs. 1a-2a a signal processing apparatus, comprising an electrical circuit (100); and a floating-gate field effect transistor (231-238) disposed in a first circuit (108) pathway of the circuit, wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit (128) characteristic in a second circuit pathway of the circuit, wherein the first and second circuit characteristics correspond to relate to transfer functions of the first and second circuit pathways.

***Allowable Subject Matter***

9. Claims 1-17, 27-32, 47, and 48 are allowed.

The prior art of record fails to disclose or fairly suggest a signal processing apparatus (as shown in Figs. 5A-5B), as recited in claim 1, comprising a time-interleaved system (96) operable to distribute a signal into a first processing pathway and, following a predetermined amount of time, into a second processing pathway; and specifically the limitation directed to a delay structure (as shown in Fig. 5B) coupled to the second processing pathway, the delay structure including at least one floating-gate field effect transistor (84 in instant Fig. 4A), wherein the predetermined amount of time depends on an amount of electrical charge (Charge Q in instant Fig. 4A) stored on the floating gate (88) of the at least one floating-gate field effect transistor, the amount of electrical charge adjusting a slew rate of an output of the delay structure to thereby controllably influence a triggering time of a circuit (99-1 through 99-m) associated with at least one of the first and second processing pathways.

The prior art of record fails to disclose or fairly suggest a signal processing apparatus (as shown in Figs. 5A-5B) and a method of use thereof, as recited in claims 4 and 13, comprising an input node configured to receive a signal; a splitter (96) operable to split the signal into a first signal portion and a second signal portion and direct the first signal portion to a first node and directing the second signal portion to a second node; and a first circuit (96-1, 98-1, 99-1) coupled between the first node and a third node, the first circuit including a first analog-valued floating-gate transistor operable to effect a time delay on the first signal portion depending on an amount of electrical charge (Charge Q in instant Fig. 4A) stored on a floating gate (88) of the first transistor (84), the amount of electrical charge adjusting a slew rate of an output of the first

circuit to thereby controllably influence a triggering time of a circuit (one of 99-1 through 99-m) associated with the third node.

The prior art of record fails to disclose or fairly suggest a signal processing apparatus (as shown in Figs. 9A-9B), as recited in claim 8, comprising a signal processing path including two or more signal processing elements (202-1 through 202-m); and a time delay element (20, and 203-1 through 203-m) disposed between adjacent processing elements of the two or more signal processing elements, the time delay element including at least one analog-valued floating-gate field effect transistor (84), wherein a time delay of the time delay element depends on an amount of electrical charge (Charge Q in instant Fig. 4A) stored on the floating gate (88) of the at least one analog-valued floating-gate field effect transistor (84), the amount of electrical charge adjusting a slew rate of an output of the time delay element to thereby controllably influence a triggering time of at least one of the two or more signal processing elements (202-1 through 202-m).

The prior art of record fails to disclose or fairly suggest an apparatus for processing a signal (as shown in Figs. 9A-9B) and a method of use thereof, as recited in claims 10 and 16, having specific structural limitations such as a first circuit (202-1 and 20) coupled between the input node (200) and the intermediate node (208-1), the first circuit including a first analog-valued floating-gate transistor operable to effect a time delay on the signal received at the input node depending on an amount of electrical charge (Charge Q in instant Fig. 4A) stored on a floating gate (88) of the first transistor (84); and a second circuit (202-2) disposed between the intermediate node and the output node (218), wherein the amount of electrical charge adjusts a slew rate of an output of the first circuit to thereby controllably influence a triggering time of the

second circuit, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest an apparatus for processing a signal (as shown in Figs. 5A-5B), as recited in claim 12, having specific structural limitations such as a first circuit (96-1, 98-1) coupled between the first node and a third node, the first circuit including a first analog-valued floating-gate transistor () operable to effect a time delay on the first signal portion depending on an amount of electrical charge (Charge Q in instant Fig. 4A) stored on a floating gate (84) of the first transistor (88), said amount of electrical charge stored on the floating gate of said first transistor adjusting a slew rate of an output of the first circuit to thereby controllably influence a triggering time of a circuit connected to the third node; and a second circuit (96-2, 98-2) coupled between the second node and a fourth node, the second circuit including a second analog-valued floating-gate transistor operable to effect a time delay on the second signal portion received depending on an amount of electrical charge stored on a floating gate of the second transistor, said amount of electrical charge stored on the floating gate of said second transistor adjusting a slew rate of an output of the second circuit to thereby controllably influence a triggering time of a circuit connected to the fourth node.

Claims 27, 47 and 48 are allowed for similar reasons; note the above discussion with regard to claims 4 and 13.

Claim 30 is allowed for similar reasons; note the above discussion with regard to claims 10 and 16.

Claim 32 is allowed for similar reasons; note the above discussion with regard to claim 1.

***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
June 5, 2005

Kenneth B. Wells
Primary Examiner